*CLAIM AMENDMENTS*

Claims 1-7 (Cancelled)

8. (Currently Amended) A semiconductor device ~~of~~ TSOP (Thin Small Outline) Package ~~type~~ having:

upper and lower semiconductor chips arranged between a first lead portion and a second lead portion ~~provided~~, respectively, on two ~~sides~~ opposing sides of said semiconductor device, in plan view ~~, comprising:~~;

a first die pad ~~portion~~ integrated with and ~~noncoplanar~~ not coplanar with said first lead portion and located ~~higher relative to~~ on one side of a reference plane passing through a central position between ~~the highest~~ a first surface and ~~the lowest~~ a second surface of said first and second lead portions; and

a second die pad ~~portion~~ integrated with and ~~noncoplanar~~ not coplanar with said second lead portion and located ~~lower relative to said~~ on a second side of the reference plane ~~; and a~~, wherein said lower semiconductor chip is supported by said first die pad ~~portion~~ and ~~an~~ said upper semiconductor chip is supported by said second die pad portion, said ~~two~~ upper and lower semiconductor chips ~~being~~ are partially ~~overlapped~~ overlapping and ~~located to~~ overlap in ~~the range of~~ height with said first and second lead portions.

9. (Currently Amended) The semiconductor device according to claim 8, ~~wherein said first die pad portion is provided to~~ including:

a first lead frame connected to said first die pad and located ~~including~~, with said first lead portion ~~above~~, on the first side of said reference plane, and

~~said second die pad portion is provided to~~ a second lead frame connected to said first die pad and located ~~including~~, with said second lead portion ~~below~~, on the second side of said reference plane.

10. (Currently Amended) The semiconductor device according to claim 9, wherein

said first die pad portion is L-shaped ~~including~~ and includes a first extension extending from an end of said first lead portion toward said second lead portion, and a first opposing portion continuing from said first extension and extending ~~in~~ parallel ~~with~~ to said first lead portion,

said second die pad portion is arranged, in plan view, opposite said first die pad ~~portion and~~, is L-shaped ~~including~~, and includes a second extension extending from an end of said second lead portion toward said first lead portion and a second opposing portion

continuing from said second extension and extending ~~in~~ parallel ~~with~~ to said second lead portion,

said first extension and said first opposing portion have ~~their~~ bottom ~~surface~~ surfaces supporting said lower semiconductor chip, and

said second extension and said second opposing portion have ~~their~~ upper ~~surface~~ surfaces supporting said upper semiconductor chip.

11. (Currently Amended) The semiconductor device according to claim 8, wherein said first and second lead portions and said first and second die ~~pad portions~~ pads are integrated into a common lead frame, said reference plane passes centrally through ~~center of~~ the thickness of said lead frame, said first die pad ~~portion~~ supports said lower semiconductor chip of said partially overlapped upper and lower semiconductor chips, and said second die pad ~~portion~~ supports said upper semiconductor chip.

12. (Currently Amended) The semiconductor device according to claim 11, including adhesive layers respectively bonding said upper and lower semiconductor chips to said first and second die pads wherein a center of the thickness of said first die pad portion and a center of the thickness of said second die pad portion are spaced ~~vertically~~ from said reference plane in respective ~~directions~~ opposite ~~to each other~~ directions, each by a distance equal to the sum of ~~a~~ one-half ~~of~~ the thickness of said lead frame and ~~a~~ one-half ~~of~~ the thickness of ~~an~~ said adhesive ~~layer~~ layers bonding said upper and lower semiconductor chips to said first and second die pads.

Claims 13-15 (Cancelled)